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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,882	10/15/2003	Kenneth Mark Williams	PA2594US	4103

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EXAMINER	
THOMAS, SHANE M	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,882	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04 & 2/24/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 10/15/2003. Claims 1-23 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Information Disclosure Statement

The information disclosure statement filed 10/18/2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Further, reference page 2 of 3 of the IDS filed 10/18/2004 has an incorrect Patent No. listed for Heybruck - Patent No. 4,893,311 is registered to Hunter et al. As such, the Heybruck reference has been crossed off and not considered by the Examiner.

The IDS filed 2/24/2006 has been considered by the Examiner; a singed copy as been included with this Office action.

Drawings

The drawings are objected to under 37 CFR 1.84(m). The use of shading in views is encouraged if it aids in understanding the invention and if it does not reduce legibility. In the present case, the shading found in figures 9 and 10 does reduce legibility of the elements contained therein.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the incrementing of a memory address pointer after a first aligned word is accessed (claims 6 and 13) and the decrementing of the memory address pointer after the first aligned word is accessed must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 13, 19, 20, and 23, are objected to because of the following informalities:

As per claim 13, the term --the next aligned word-- should be amended to --a next aligned word-- as --*the* aligned word-- has not been previously defined in the claims.

As per claims 19,20, and 23, it is not readily apparent to the Examiner if the Applicant purposely meant to phrase that the --specified number-- is stored "**as**" an [first] index (as claimed), or instead, meant to claim that the --specified number-- is stored "**at**" an [first] index. Paragraph 75 of the Applicant's specification as originally filed seems to support the Examiner's suggestion. The Examiner shall interpret claims 19,20, and 23, as such.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 17-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 17-23 are not limited to tangible embodiments. In view of applicants' disclosure, specification - paragraphs 66-82, no appropriate medium to realize and contain the GET (claims 17-20) and PUT (claims 21-23) instructions is taught or mentioned; an appropriate medium is not realized in the claims in which the instructions are contained. As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 17-23, Applicant claims a single GET (claims 17-20) or PUT (claims 21-23) instruction performing the respective steps of the claims; however, Applicant clearly teaches in ¶¶72-93 and figures 9 and 10 that *multiple* GET/PUT instructions of various types are executed to perform the implementation of the steps of the claims. For example, referring to

figure 9, GETINIT instructions are used to initialize the load/store buffer by loading first and second aligned words (Steps 905 and 915, corresponding to lines 3-6 of claim 17), while GET 7 and GET 8 instructions (Steps 925 and 935, corresponding to lines 7-8 of claim 17) are used to read the "one or more" data sequences from the load/store buffer. A similar example can be seen with respect to figure 10 regarding the use of *multiple* PUT instructions.

As such, the Examiner has interpreted the GET and PUT claims 17-23 as comprising multiple instructions, rather than the single GET or PUT instruction, to perform the claimed steps.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,5,6,8-10,12,13, and 15-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Petersen (U.S. Patent No. 5,517,627). Further the prior art reference of Voith et al. (U.S. Patent No. 5,636,224) is being used to support an inherent feature of the Petersen reference.

As per claims 1,15, and 17, Petersen teaches a **method** (figures 10 and 13), **system** (figure 8), and GET (read) and PUT (write) **instructions** (write and read aligners can be implemented with a ROM, which is well known in the art to contain instructions for controlling

hardware systems, - [13/7-11]) for **processing data sequences of arbitrary length in a computing system**.

Petersen teaches **initializing a load/store buffer** (data aligner 24, figure 8) **by loading a first aligned word of fixed length** (4 bytes - [7/55-63]) **into the load/store buffer** (figure 5A - [8/41-47]). The Examiner is considering loading a data word from the buffer 27 to the data aligner 24 as --initializing-- since the process places data into the data aligner. It can be seen with respect to figures 5A and 5B that it takes two loads to the data aligner 24 from the buffer memory 27 to --initialize-- the data aligner by placing data therein.

Further, Petersen teaches **further initializing the load store buffer** 24 **by loading a second aligned word** (figure 5B) **into the load/store buffer** [8/48-50], **reading one or more data sequences** (wherein a single data sequence is being defined by the Examiner as the number of bits transferred per lane L2(i), in the present embodiment of Petersen - one byte (8 bits) - [7/55-63]) **from the load/store buffer, such that the total length of the sequences in each read does not exceed the fixed length of the first aligned word** ([8/30-58] which states that a full-width read is 4 bytes - [8/56-57]), **and loading additional aligned words to the load/store buffer to replace data sequences that are read** ([13/51/54], where the reading process can be repeated as necessary to read data from the buffer memory 27 - [figure 13, step 153 - step 142]).

As per claim 2, Petersen teaches that **the data sequence length** [read] **is a byte** [8/42-43] and [7/60-61].

As per claim 3, Petersen teaches that **the data sequence length** [read] **is a bit** [7/64-67].

As per claims 5 and 12, Petersen teaches **wherein the computing system comprises a general-purpose processor** [host processor 10] - figure 7.

As per claims 6 and 13, Petersen inherently teaches **wherein the first aligned is stored in a first memory location and the second [next] aligned word is stored in an adjacent second memory location** (the aligned words are stored in a FIFO [10/12], so as well known in the art and an inherent feature of Petersen, a FIFO buffer stores a subsequent piece of data in an adjacent location to the location of the previous piece of data - refer to figure 3 of Voith), **and the second memory location is accessed by incrementing a memory address pointer after the first aligned word** (a further inherent feature of a FIFO, since a write pointer must be incremented to the next memory location after data has been written to a present FIFO memory location - refer to Voith figure 4 and [5/63-66]).

As per claims 8,16, and 21, the rejection follows similarly to the rejection of claims 1,15, and 17. Petersen teaches **initializing a load/store buffer** (data aligner 24) **with one or more unaligned data sequences** [4/22-61], **such that the total length of each data sequence does not exceed the fixed length of an aligned word** (i.e. 32-bit word) [6/53-7/25] and figures 4A-4C. It should be noted that the Examiner is consider the step of write initializing to be the step of simply writing a first data sequence to the data aligner 24, such as the writing of data **01** in the data aligner 24 (as shown being queued in figure 4A - [6/53-55]. Further, Petersen teaches **writing one or more unaligned data sequences to the initialized load/store buffer** 24, **such that the written unaligned data shifts an aligned word into a memory location** (into the buffer 27) - figure 4B and [6/59-63]. Finally, Petersen teaches **flushing of the load/store buffer** 24 **in order to store any of the remaining unaligned data in order to store any of the remaining unaligned data into memory** (figure 4C and [6/64-7/4]). Figure 4C and [6/64-7/4] teaches that the unaligned data 01,02,03, and 04, now configured to an aligned word, is flushed

(i.e. sent to the buffer 27 as taught above) while remaining unaligned data 05 is stored into memory (i.e. the queue(s) of the data aligner - [7/1-4].

As per claim 9, Petersen teaches that **the data sequence length** [written] **is a byte** - figure 4A, [6/53-59] and [4/7-10].

As per claim 10, Petersen teaches that **the data sequence length** [written] **is a bit** [4/9-10].

As per claim 18, Petersen teaches that **the number of data sequences read is an immediate specified number** that is specified by the host [8/62-67].

As per claim 19, Petersen teaches that **the number of data sequences read is a specified number stored at an index in a register memory** [9/4-6].

As per claim 20, Petersen teaches **in which a first one of the one or most data sequences read is located at a first memory location** (i.e. any of the bytes of the 4 byte word entry of FIFO buffer 27 that is first read into the data aligner upon a read request from the host - [8/41-46] that initializes the data aligner as discussed supra) **and the one or more data sequences comprises a specified number of data sequences stored in a register memory** 27 (here the Examiner is considering the buffer memory 27 as being the register memory and the --specified number-- of data sequences stored at the first index of the [FIFO] buffer 27 is specified to be four - as each [FIFO] buffer 27 entry contains four data sequences (four aligned bytes) - [1/26-35] and [8/30-50] - where the --first index-- is the index of the first entry of the FIFO buffer 27 to be read), **wherein the subsequent data sequence following the first of the data sequences is located at a second memory location pointed to by a second index** (the

next memory location that is accessed from the FIFO buffer 27 - [8/48-50] as taught in the following example).

Petersen teaches that the first data sequence read can be any of the data sequences of the first FIFO buffer, with data unit 01 being used as an example that is read first [8/41-47]. If for example, the 04 data sequence was read first (i.e. the --first of the one or more data sequences--), thereby leaving data sequences 01,02, and 03, in the queues of the data aligner, data sequences 01, 02, 03, 05, 06, 07, and 08, would have been available to the host [8/51-52]. Thus it can be seen that the **subsequent data sequence** (data sequence 05) **following the first of the data sequences** (04) **is located at a second memory location** (buffer 27, second entry) that is **pointed to by a second index** (i.e. whatever the index/address of the FIFO buffer 27 contains the next data word that is read after the first data word - [8/48-50]).

As per claim 22, Petersen teaches **the number of unaligned data sequences written is an immediate specified number** that is specified by the host [5/41-46], in similar fashion to the number of requested data sequences read [8/62-67].

As per claim 23, Petersen teaches that **the number of unaligned data sequences written is a specified number stored at an index in a register memory** where the --register memory-- is the combination of the registers S1(0) through S1(N) [6/16-20] with each register indicating that an unaligned data sequence is stored in the respective queue. In other words the specified number is an index since the registers S1(0) to S1(N) need to be indexed to acquire the number of unaligned data sequences that are queued in the data aligner 24 from a previous write request; these indexed registers (collectively a --register memory--) combine to produce the CURRENT QUEUED value.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen (U.S. Patent No. 5,517,627) in view of Emma (U.S. Patent No. 5,619,665).

As per claims 4 and 11, Petersen teaches a general-purpose processor (host processor 10 - figure 7) but does not specifically teach a **processor having an extensible instruction set**. Emma teaches in the abstract that extension of an instruction set allows for circumventing software compatibility issues when allowing legacy software to benefit from new architectural extensions without recompilation and reassembly. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the data aligner system of figure 7 of Petersen with the teaching of an extension instruction set of Emma in order to have gained expandability of the instruction set of the processor 10 of Petersen, thereby gaining flexibility and compatibility for future instruction extensions without having to recompile or reassemble the system of Petersen.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen (U.S. Patent No. 5,517,627) in view of Voith et al. (U.S. Patent No. 5,636,224).

As per claims 7 and 14, the rejections of lines 1-2 follows the rejection of lines 1-2 of claims 6 and 13, respectively. Petersen (with Voith as a supporting reference) teaches that the claimed invention inherently uses incrementing of an address pointer to access a second memory location instead of decrementing the address pointer to access the second memory location. Voith teaches **that the second memory location is accessed by decrementing a memory address pointer after the first aligned word is accessed** [6/35-43] is an equivalent method known in the art of FIFO accessing. Therefore, because these two method of accessing a subsequent memory location in a FIFO buffer were art-recognized equivalents at the time the invention was made, one of ordinary still in the art would have found it obvious to substitute decrementing a memory address pointer for incrementing a memory address pointer of a FIFO buffer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

HONG CHONG KIM
PRIMARY EXAMINER